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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte GERALD K. BARTLEY, WIREN DALE BECKER, ANDREAS HUBER, and TINGDONG ZHOU

Appeal 2019-005219 Application 15/057,622 Technology Center 2800

Before CATHERINE Q. TIMM, JEFFREY T. SMITH, and GRACE KARAFFA OBERMANN, *Administrative Patent Judges*.

OBERMANN, Administrative Patent Judge.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant¹ appeals from the Examiner's decision rejecting claims 12–22. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

¹ We use "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as International Business Machines Corporation. Appeal Br. 2.

STATEMENT OF THE CASE

The claims relate to a method for making an integrated circuit package for optimizing power distribution. Spec. 1:1–2:2, Claim 12. "Microelectronic components are continually being miniaturized" and, presently, the "technology has advanced to the point that three dimensional chip stacks" incorporate "conventional C4 solder ball arrays, then Through Silicon Vias (TSVs) in an intermediate integrated chip from which the power is transmitted through smaller, i.e., micro uC4 solder ball arrays," which "power up integrated circuit memory and logic areas or cells." Spec. 1:11–17. The Specification explains, "Because the uC4 interface uses smaller C4 balls and has a high percentage of tin material to improve the reliability of the interface, that interface is subject to high electro-migration (EM) concerns." *Id.* at 4:12–14. According to the Specification, "if the coincidence of the micro C4 solder ball and the vias in the TSVs are [offset] so as to eliminate or at least minimize the coincidence of micro solder balls and vias, the electro migration problem . . . is minimized." *Id.* at 4:27–29.

Claim 12 is illustrative of the claimed subject matter and states:

12. A method for making an integrated circuit package comprising:

forming a first grid array of C4 solder balls on a substrate having conductive interconnectors, said solder balls being respectively connected to the substrate interconnectors;

mounting a first integrated circuit chip including TSVs (Through Silicon Vias) on said grid array of C4 solder balls, said chip having a conductive connector grid pattern coincident with said grid array of C4 solder balls wherein said integrated circuit is connected to said conductive interconnectors in said substrate;

forming a second grid array of C4 solder balls on the upper surface of said integrated circuit chip connected to conductive Application 15/057,622

interconnectors on said upper surface of said first integrated circuit chip; and

mounting a second integrated circuit chip mounted on said second grid array of C4 solder balls wherein said second grid array of C4 solder balls connects conductive connectors in said second chip to said conductive interconnectors on said upper surface, wherein

said C4 solder balls in said second grid array are offset so as not to horizontally coincide with TSVs in said first integrated circuit chip.

OPINION

The Examiner rejects claim 12 as anticipated by Lin² and claims 13–22 as obvious over Lin. Final Act. 2–8.

Rejection of claim 12 over Lin

The Examiner finds that Figure 11A of Lin teaches "C4 solder balls" that are "offset so as not to horizontally coincide with TSVs." Final Act. 4. The Examiner explains that "the phrase 'not to horizontally coincide' means not perfectly lined up," and that "[a]ny structure not perfectly lined up would meet this limitation." *Id.* The Examiner concludes that "Lin's teaching of off-center meets this interpretation." *Id.*

Appellant disagrees, asserting that "Lin fails to recognize the problem addressed by this invention or the claimed novel solution." Appeal Br. 6. Appellant acknowledges that, "[w]hile balls 38 do not exactly coincide with vias 24, all of the balls 38 do respectively coincide with a via 24." *Id.* at 7. Appellant further argues that, "[i]f one applies a straight edge vertically to Fig .1, they will find that a portion of each ball 38 horizontally overlaps a

² Lin et al., US 2013/0134559 A1, published May 30, 2013.

via 24," and that "[t]he minimal offset from an exact alignment is only a result of [Lin's] metallization pattern." *Id.* at 7–8.

During patent prosecution, the Office assigns claim terms their broadest reasonable interpretation consistent with the specification. MPEP § 2111. "The broadest reasonable interpretation does not mean the broadest possible interpretation." *Id.* "Rather, the meaning given to a claim term must be consistent with the ordinary and customary meaning of the term (unless the term has been given a special definition in the specification), and must be consistent with the use of the claim term in the specification and drawings." *Id.* Consistent with that guidance, the Examiner reasons that "the phrase 'offset so as not to horizontally coincide' does not necessarily mean there is a complete offset of the C4 balls without any overlap whatsoever." Ans. 3. In other words, the phrase at hand reasonably "can be interpreted as meaning they do not exactly horizontally match up and do not occupy the exact same horizontal space." *Id.*

We agree with the Examiner. Appellant identifies no persuasive reasons for narrowing the disputed claim term to exclude all horizontal overlap. Further, the Examiner's interpretation is consistent with the Specification, which indicates that "the coincidence of the micro C4 solder ball and the vias in the TSVs are [offset] so as to eliminate or at least minimize the coincidence of micro solder balls and vias." Spec. 4:26–29. This guidance in the Specification – that the offset contemplated by claim 1 will "at least minimize the coincidence" – supports the Examiner's view that the term "offset so as not to horizontally coincide" embraces a configuration in which partial horizontal overlap is present.

We find Appellant's assertion that "Lin fails to recognize the problem addressed by [the instant] invention or the claimed novel solution"

inadequate to demonstrate reversible error. Appeal Br. 6. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989). Anticipation does not depend upon, or even take into account, whether or not the prior art reference recognizes the same problem set forth in Appellants' Specification.

For the above reasons, we maintain the Examiner's rejection of claim 12.

Rejection of claims 13-22 over Lin

Regarding the Examiner's obviousness rejection of claims 13–22 over Lin, Appellant relies on the same arguments set forth as to independent claim 12. Appeal Br. 8.³ We affirm the rejection for the reasons stated above regarding claim 12.

³ Appellant misidentifies the rejected claims as claims 1–11 in the final paragraph of the Argument section of its brief, but correctly identifies the claims at issue as claims 12–22 in the Conclusion section. Appeal Br. 8.

CONCLUSION

We affirm the Examiner's decision to reject claims 12–22.

Claims	35 U.S.C.	Reference(s)/Basis	Affirmed	Reversed
Rejected	§			
12	102	Lin	12	
13–22	103	Lin	13–22	
Overall			12–22	
Outcome				

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1).

AFFIRMED